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Ltspice simulation online

Please send your requests to additions or changes in LTSPICE not documented in the "Discussion" page (second guide above). LTSPICE / SWITCHCAD III is a complete and fully functional spice program (Electronic circuit simulator) available for free from the linear Technology Corporation (LTC). Because of its superior performance, excellent support to community and ease of sharing files, it is rapidly replacing all other spice programs, regardless of the price, as the simulator of choice for hobbyists, students and professionals. The objective of this topic is to explore and explore some of the many useful or peculiar characteristics that have never appeared in the standard documentation if due to the simple supervision, the resource considered is not important enough, no the polite enough or functionally obsolete "or even due to the appeal being considered the owner for another brand of spices or for the own LTSPICE. LTC considers some of these indocumented features as a fair game for open discussion in Public Furins Group of LTSPICE

Yahoo users, while for others, considers that such discussions open as a violation of their licensing contract. "Fair game" is any characteristic or was already part of the distribution Normal, that is, it appears or has appeared in the help file, such as simple text in any of the sample or example files, on any program menu available during normal program use, or any of the Enterables, presentation files or leaflets of any presentation of LTSPICE seminars. Such items are officially considered "documented" and are specifically permitted as discussion topics in public drugs such as the LTSPICE group of Yahoo users. However, it is advisable that all items that have been discarded from the documentation, even if they still work, generally should be considered obsolete and at risk of being expurgated from the program's code at any time (fortunately, these items are quite raw). As for the classification of anything not covered above, you should make your own judgment of common sense or ask the Board of the Moderator of the Group of User Group or the author of the Private E-mail program. Clearly any genetic spice feature that works in LTSPICE would be OK for general use and discussion, regardless of their documentation state in Ltspice . Many of the standard devices have indocumented parameters (for example , Tempts) or syntax (for example, specific compatibility of PSPICE) that would fall into this category. Only as clearly, any specific indocumented device for the encrypted LTC models, high-performance IC models would probably be considered the proprietary knowledge to be protected with due diligence of the release for the public domain, Competitors for LTC, LTC competitors earn the permission in fact to copy them freely in their own circuit simulator offers (however, it is difficult to see how LTC could legitimately prevent private individuals Use of characteristics as undocumented in their own simulations or discussing them through private communications). For these reasons, this last category of indocumented features will not be directly discussed here. NUMBER NUMBER / RICE RICA LTSPICE usually represents numbers using 64-bit double accuracy arithmetic with the following data structure: for LTSPICE general component values accept numbers ranging from magnitude of $\tilde{A} \sim 1,798 \times 10 + 308$ small small as $\pm \tilde{A} \pm 2,225 \times 10508$. $\tilde{A} \tilde{A} \tilde{A} \tilde{A} \sim$, the values that exceed this interval are interpreted as infinite or zero. However, due to the need for 52 bits of the fractional part of the significant, the practical the dynamic range numms will be dependent on the A binary meaning of 53-bit for the LTSPICE about 16 significant figures for internal mathemetic computations. Thus, if the impedances vary by more than 16 orders of magnitude, numerous difficulties can follow, depending on the topology of the circuit (ie because the matrix solution frequently involves differentiating two two $\tilde{A} \epsilon \tilde{A} \epsilon$ "For example, the nearest number of more than one is 1.000000000000002 - anything closest is not solved). LTSPICE's alternate proprietary solver extends this precision for about 3 more Greatness orders at a cost of a modest speed penalty. A-Devices A-Devices are the elements of special circuit-circuit-circuit feature of linear corporation technology. According to With the LTSPICE help file, the behavior of a number of these is indocumented because they often change with each new set of available models for LTSPICE (such changes really are very rare and this is more likely offered as as much as a credible reason to keep them hidden and to discourage no one to worry about trying to explore and / or use them). The help file list the syntax A-Device as: Annn N004 N002 N003 N004 N005 N003 N004 N008 N006 N007 N008 [Model> [Model> [Model> [Model> [Instone ϵ n CIA Parthrets] Note that all AT devices may actuate active devices, until 5 inputs (terminals 1 to 5) usually two outputs (terminals 6 and 7), and terminal 8 whenever the Common device.A, A-devices are always netlisted with the total number of eight connections.â NetLister connects any entries and outputs not used for terminal 8.AA A -Device compiler recognizes this condition As a flag that this terminal is not used and removes it from the simulation matrix. The chain is originated or sunken from the outputs (usually the q or main outer in terminal 7 and the complementary output at the terminal. 6) and is returned through the common device, terminal 8. A-devices are implemented way to allow a single device type to act as any combination of a 1 to 5, 1 to 2 output device, but without simulation speed penalty for terminals not used . Refer to the LE program help program for more details on documented LTSPICE devices. Here is a listing of all known LTSPICE devices A. Documented directly in Help: BUF (AKA BUF1 INV) E or XOR - When more than two inputs are present, it uses the correct definition of True One and only one entry is true, instead of the most common incorrect definition of true if a number of inputs is true (which must be called the ompar / nodd gate instead of a gate XOR / XNOR). Schmitt (AKA Schmittbuf Schmittinv Difrschmitt Difschmittbuf diffschmittinv) DFLOP (CLR has precedence over the premise, also a starting state can be set $\tilde{A} \epsilon \tilde{r} \sim$ "see srllop) varistor modulator (modular modular aka2) not documented in Help, but available through the schematic component selector: srllop - Located in Digital Phasedet (also known as Phidet) "Located on the Digital Balcony" located in Digital and documented in the Group of User (was Officially approved for public use) Samplehold (sample) "Located in special functions documented in sample schemes included in the distribution of the program: Phasedet (also known as Phidet)" Located in Examples / Educational / PLL2. AC Samplehold (AKA sample) "Located in Examples / Educational / S & H.asc OTA" Used in Subcircuits Simple text Universalopamp (in lib / sub), but group messages of users (some long-standing) containing information on aspects of this were censured not documented anywhere by LTC: xxxxxxxx a before long date pos group users on this digital alternating type device has now been censored xxxxxxxx $\tilde{A} \epsilon \sim$ "DAC type device never Discussion in the XXXXX User Group "DAC TYPE Device never discussed in the XXXX User Group" DAC TYPE Device never discussed in the XXX user group - Amplifier type device has never discussed in the user group not documented anywhere in LTC, but Two first of these devices were widely documented in the group of users. All three devices that were executable from LTSPICE Executable: JKFLOP PGATEDRIVE INVPGATEDRIVE INVGATEDRIVE Three DACs, xxxxxxxx, xxxxxx, xxxx, are specialized to devices that are likely to be a little general interest (although their functions and Pinouts could probably be easy to guess by examining the few LTC ICS specialized data sheets making use of them). XXXX seems to be the only simple DAC, genital, but very spices-efficient DACs are very easy to do using standard, approved devices. SRFLOP The set / reset Flip-flop symbol is located in the digital symbol folder. The input (reset) R takes precedence over (set) of input S. The start state of the flip-flop (initial condition) can be determined by adding an "IC = " attribute. An "IC" value interprets Ref for a high level, for example, defines the high exit "IC = 1" q and "ic = 0" define low.â (Note: The Lipstick Ref Parthrets Patterns for 0.5 and its use is documented in help.) Phasedet (AKA Phidet) The phase detector is located in the digital symbol folder. Examples folder contain a scheme with some documentation: Examples / educational / PLL2.asc Samplehold (aka sample) Sample & symbol is in the FUNCTION FUNCTIONS Special symbols. An schematic example, S & H.asc, is situated in the schematic examples / educational. The behavioral and hold device sample has two modes of operation. A skim can accompany the entry when the S / H input is true or the output can latch for the input when the clk input goes true. , Note that one and only one of these two entries must be connected. Senic parameters for sampling and retraining the following are the following: standard rout for 1rs A ϵ (instead of to a standard device 1a). VHIGH and VLOW 10V standard pattern for -10v (note: these are the outlit tensile saturation levels). The OTA OTA (operational transconductance amplifier) is used in the various Sub-circuits universalopamp of plain text (located in a standard LTSPICE program in lib / sub). The standard transfer function is a hyperbolic tangent (TANH), which closely closely closer to the transfer function of a difference bipolar transition amplifier (this limit may be disabled by the addition The Linear flag parameter. The two differential input pairs are available in pins 1 and 2 (A +) and on pins 3 and 4 (+ a). The above appears from the current source of Transconducture in pin 7.A as usual, pin 8, if connected, becomes floating reference "GND" of the device. For reference, a CC "rail" voltage, which represents the possible maximum output (calculated from the combination both the current and tension saturation limits) appears on the pin 6 .A this tension reflects only the negative limit and has an identical depletion remedy to that of the main skirt. Parthrets (* indicates a non-documented parameter) A note of all the parameters of Ota were not documented to November 2019, Ref (Pattern = 0V) is the offset of tension input g (pattern = 1U-MHO) is the gross "gain" input (transconducton), where VDIFF = (Ref a $\tilde{V} (1,2)) * \tilde{V} (3,4)$) AE IRAW = L * VDIFF IOU (default = 10UA) is the output saturation current, which can be replaced by one or both ISRC (or ISRC, standard = IOU) is the Saturation Saturation Supply Isink (a Negative Number, Pattern = $\tilde{A} \epsilon$) Oout) is the Saturation Saturation of Current Saúda ASYM is a paramount flag that, if present , allows independent asymmetric limits for ISRC / Source and Isink linear is a flag parameter that, if the output present, limiting * IOFFSET (default = 0a) is the current outset * PowerUp (Pattern = True) is a Boolean parameter that if) where is the expression assigned to this compulsory parameter. Duty specifies the width width = round (cycles * duty). Defaults work cycle for 0.5 if omitted. Most of the parameters of a usual digital device can also be applied, optionally, for example, trise, vhigh, vlow, ref, etc., with the exception of td, which is ignored (The counter accepts no delay). Expression cycles accepts B-source syntax and therefore can be a simple constant or can be a constant-containing expression complex, parameters, functions, the keyword time, tensions of n° branch currents.â, the accountant goes to zero whenever the cycle value falls below 1.5.â, if the counter is timed when the cycle value is less than 1.5, the counter is restored. To use this parametable cycle symbol should be specified after you place the symbol in a schema (right-click on the symbol to open the "Attribute Component Editor" window, and in the Value Attribute field, type a param Metro cycles, for example, "cycles = 2" for a division for two counter). A symbol including the entry and reset test circuit is available in Yahoo Ltspice Group of users Files / TUT / Digital A-Devices.An, Alternative, S / R LTSPICE Flip-Flop Symbol Can be used to replace the counter with reset Editing your "srllop" SpiceModel attribute to "Counter" after being Placed in the scheme (S Become the Right Religi R becomes the entry of redefinition and q and q q $\tilde{A} \sim$, become the two outputs). B-fonts Although many B-font features have not been documented in relatively recently (~ 2007), most are now at least played in help and the few who are not covered in fonts B (Complete reference) In this wiki. CPAR, in addition to the RPPAR parameter (which is documented in help), behavioral fonts of the current source type (ie "I = "r =" and "p =") now accept the CPAR paramet to specify a parallel capacity. Sources B derivatives, driving an ohm in parallel with a small capacitance (for example, rpar = 1 npar = 1n) are much more friendly friends than the fonts of struggling voltages and should be used whenever possible. Nortonizing tension fonts for the current sources in parallel Ohm does not require conversion calculation, but Nortonized parallel impedance can be adjusted as low as desired if the current source gain is scaled compensate. Bn p = f (...) join / arbitrary source in which f is a constant function or is an arbitrary function of any tension of node vascular, Ramifying current, etc. As with fonts b pattern (note: the energy is provided when f is negative). To avoid large current in zero-to-zero tension, the power sheets / arbitrary energy sources to withstand resistive behavior when the absolute value of the voltage throughout the device falls below a standard value of 1 volt. Modified Specifying a VPRxover parameter for the device, for example VPRxover = 50MV. Bn r = f (...) arbitrary resistance, where f is an arbitrary function of x (which has the special meaning of the r-voltage in this context) and / or any voltage of Node, branch chain, etc. fonts b pattern. [[Units] Freq = [Delay =]] The transfer function of the Freq circuit element is specified by an ordered list of freq points (Hz), MAG (DB) and Phase (C) as follows: where F1 View) Show list boxes in the schema when a role is moved. Creating a label when making a DC (.op) operating point simulation, a data label from the operation point can be created As follows run the left .op simulation click on a network (a wire). This creates a new label that can be placed with the cursor. Creating a label by making another simulations when doing other types of simulations than a dc (.op) operating point simulation the operation point data rotles can be created with the right mouse button in an empty area of the schema and then selecting Place. Data label on the drop-down menu. The new label can be attached to a network with the cursor. Format and layout Once placed, a operating point data label can be moved freely or copied and then edited to be completely not related to the original node. Of course it is possible as possible A rigus using normal drawing functions. For example, painting a rectangle around it (Main Menu Edit-> Draw-> Retain) or by placing some close text (main menu). Standard operating point data tags for the tension display of the n° to which they are connected (meanings by the "S" cipher character), but this can be edited to be any varying expression, including currents, powers or even the tension of a specific knot. By clicking with the right mouse button on an operating point data label brings a pop-up window to select the data to display or enter an expression. With fractions, all available non-zero dips are displayed, often resulting in an unwanted numeric disorder. The number of visible dies can be aesthetically limited, properly editing the expression. Examples of rounding expressions used for formatting: (8 1k) / 1k ϵ ; Display no more than 3 dips (usually selected automatically in engineering format). Round (I (R1) * 1k) / 1k ϵ ; The same display format above, but the expression is the current through R1. Round (V (1,2) * 1k) / 1k ϵ ; The same format, but the expression of the tension difference between the 1 & 2 . Bussing connections and components (bushography notice) LTSPICE has an indocumented resource to draw Negotes (Network Groups) in the schema. This feature is erratic. It is recommended to check the resulting circuit by studying Netlist (main menu view -> Netlist of spices), because it is possible to attach wires to bus without knowing which sign (liquid) of the bus the wire should actually represent . The buses are purely cosmetic in the scheme, they do not have special function of spices. All Bussing notice is settled (flattened to normal liquid notice) by the schematic editor before the creation of spices netlist (Netlistser does not understand the notice Bus, that is, it is not possible to use a spice deck with noibus in LTSPICE). An alternative to the bus is to use individual liquid labels to connect distant networks. A network (wire) becomes a bus whenever any of the three conditions below are answered: the wire is labeled with a NetName with a matrix suffix. A matrix suffix consists of two numbers separated by a cyclon and closed between paragraphs. Example of data [0: 7] means that the bus consists of the eight network data [0], data [1], until data [7]. The wire is connected to the wide end of a bus bus (Main Menu Edit-> Place the TAP bus). A network connected to another end, the pontiards of a faucet, is called the faucet network, and is an individual network from the networks represented by the bus. Faucet networks should be labeled with an individual matrix element suffix (a single numberless numberless number included in paragraphs). For example, data [3] would be the role of a faucet network off the data bus [0: 7]. The network is connected to a bus pin from a component that has a matrix type name. Once a wire is becoming a bus, it is automatically drawn with thick extra lines. A bus can be automatically connected (netlisted) to a corresponding matrix of components. An array of components is created by attaching a array specifier from brackets to the name of the instance (reference designatory) of a single-connected bus component. For example, naming a Q1 transistor naming it [1: 4] would result in the single symptom that represents four identical transistors. The base pins, collector and issuer of these matrix of components need to be connected to bus. For example, for busy buses base [1: 4], collector [1: 4] and issuer [1: 4]. The resulting Netlist is arbitrary if the pins of an array of components are not Connected correctly to busses, but for example, accidentally for unique networks only. Note that recursive connections are possible around a single device or group of devices by use appropriate liquid labeling. In the example , a single digital dclop device can be annotated to represent a 64 Shift-registrar string by: Adding a suffix of 64 elements to its instance name, for example A1 would become A1 [0:63], [0:63]. In its D input a corresponding label matrix network, for example, data [0:63] (name in the particular $\tilde{A} \epsilon$ important), and placing its output Q in a network label substituaAa appropriately, for example, data [1:64]. The result would be that the A1 inputs D [1] to A1 [63] is connected to the s $\tilde{f}$ Q outputs A1 [0] to A1 [62]. The D input A1 [0] [Data [0]] eq Output A1 [63] (data [64]) must be played individually from the bus and represent the input and output of the resulting 64-bit shift register . Example Notes: As usual for any flip-flop, one for delay ϵ meter must be specified in the value field, e.g., TD = 10ns. The D input to the door first $\tilde{c}$ can be accessed individually by their Andrice appropriate matrix, for example, data [0] The title esquemÃtico block editor can display a special sÃmbolo as a title block. This $\tilde{A} \epsilon$ a combined resource esquemÃtico and Symbols Editor editor. The feature $\tilde{A} \epsilon$ Cosma purely optical. Lets decorate a esquemÃtico so that more pareÃsa a traditional design (depending on what $\tilde{A} \epsilon$ actually sÃmbolo in the title block). The title block must be created as a sÃmbolo (.asy file) and be master of the kind of sÃmbolo. However, the editor Symbols the LTSpice nA $\tilde{f}$ allows creating the sÃmbolo with such a type, such as editing sÃmbolo $\tilde{A} \epsilon$ possible. So $\tilde{A} \epsilon$ initially Necessary create an empty master sÃmbolo with a text editor. Once initially created initially, can be opened and edited in LTSpice. To start $\tilde{A} \epsilon$ enough to create a file with .asy the two lines below in a text editor Version $\tilde{f}$ 4 Symboltype Master once saved the text editor The file can be opened in LTSpice and drawing commands can be $\tilde{a}$ used to design the title block, for example a table, and vÃrios text fields. The pins on the $\tilde{f}$ should be added to a sÃmbolo the title block. Once saved in the directory of the project, the title block can be added to such a scheme as any other sÃmbolo. As $\tilde{A} \epsilon$ edit a difficult esquemÃtico while a title block $\tilde{A} \epsilon$ Visible (trying to select a component results in $\tilde{f}$ Selecting the title block), the title block can be turned on and off atravÃ $\tilde{A} \epsilon$ s as follows Opa \$Receiving\$ the $\tilde{f}$. View-> Control Panel> Using Option RedaÃÃ $\tilde{f}$ ϵ Show title block Before you print a page with a title block, $\tilde{A} \epsilon$ advisable to adjust the layout of the zoom in the editor esquemÃtico optical, so that the scheme with the title block fits exactly on the screen. This can be done atravÃ $\tilde{A} \epsilon$ s button $\tilde{f}$ the tools "complete extensive zoom" bar or menu item View-> Zoom to fit. This pressupÃpie each sÃmbolo was designed within the limits of the title block. Here estÃj an example of a file sÃmbolo simple title block: Item Title-block.asy. Symbols editor putting linear technology or both analog devices logos within a sÃmbolo, LT or ADI text (must be all maiÃsculos) in a sÃmbolo (Draw- menu-> Text) $\tilde{A} \epsilon$ overridden by the corresponding company logo when sÃmbolo $\tilde{A} \epsilon$ used in a scheme. Cut and paste between Symbols Unfortunately, this has yet to be implemented. Two alternative SÃ $\tilde{f}$ o Possible Solutions but sÃ $\tilde{f}$ both the incÃmodo. Open sÃmbolo that you want to copy. Enta $\tilde{f}$ immediately salvÃj it with a new name. Modifying first before saving $\tilde{A} \epsilon$ dangerous because it requires always remember to change the name of a process aft the ediÃÃ $\tilde{f}$ distracting. However, if the original is inadvertently overwritten, as long as the sampler file the $\tilde{f}$ is closed, the original can be recovered by repeatedly pressing the Undo button and then recovering. Use a text editor to open Symbols files and copy the drawing command sequÃncias ASCII from one file to another. NA commands the $\tilde{f}$ sÃ $\tilde{f}$ difÃceis the reading for $\tilde{f}$ ediÃÃ the selective, but the whole seqÃ¼Ãncia Tamba $\tilde{A} \epsilon$ m can be copied and Clean graphically from within the LTSPICE symbol editor. Plot of the cross-polling key combination Click on ALT-LEFT in a role in the plot panel highlights the corresponding node in the schema (since the end of October 2012). E.g. Click on ALT-LEFT on a label like V (N001) on the plot panel highlights the N001 n°. Clicking Alt-Left Alt-Left A LIKEI mark (R1) highlights R1 in the scheme. The LTSPICE eye diagram can trace ocular diagrams - a resource that is only semi-documented. The following menu items "Plot Settings" related to ocular diagrams (select a Plot Panel (RAW)) Plot Settings-> Enable Diagram-> Enable Plot Settings-> Eye Diagram -> Properties that they are usually disabled. LTSPICE allows them when adding the Baudrate-Option option insufficiently documented = for a schema. Instead of the nominal symbol rate of the signal must be given. "Rate"> Defines in which ranges The signal must be triggered. Once you allow the plot Settings-> The ocular diagram menu item-> Properties allows you to set two more properties of the eye diagram. An initial delay, which effectively specifies where the eye (s) should be plotted on the horizontal axis. And the number of eyes, which are equivalent to how many shooting intervals should be displayed. The following schemes, both contain a Baudrate option, but it is Reviewed. Examples / Education / PLLAC Examples / Education / PLL2.ASC Betting the option, running the simulation, allowing the ocular diagram in the plot configurations and then probing the signal network (no network outside) gives a typical eye diagram. Subcircuit waveforms (signal name conversions) to display waveforms of subcircuit, you must first ensure that the non-dry subcircuit voltages and the options save subcircuit devices currents Be enabled on the Save Patterns tab. Then if your the simulation was created as a hieracich design using the LTSPICE schematic capture window, you can simply use the probe tool to select an active subcircuit scheme according as you need River. But if Spice Netlist was imported from an external source, the format of the SPE instruction is the following: .probe v (n°).probe v (subckt name: n°).probe v (subckt name: n°) A MOSFET Subcircuit Drainage: .Probe ID (SUBCKT_NAME: MP1) NETLIST A NETLIST line starting with "!. LTSPICE." It is now treated as a spice directive for LTSPICE (but a comment on others Spice programs). - 09/05/06 $\tilde{A}$, $\tilde{a} \epsilon$ ceThe spice versions have no such problem with the comments of the time blog fed by

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